Possible Future instrumentation upgrades

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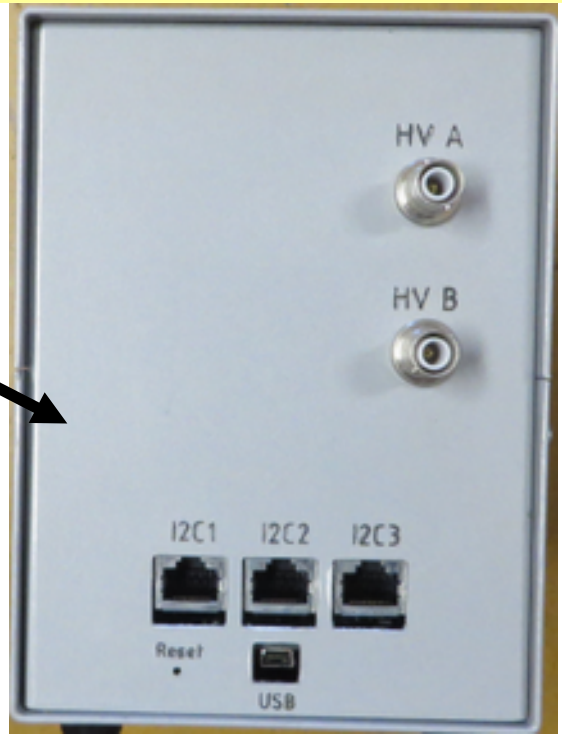
III TRAGALDABAS Collaboration meeting
Santiago of Compostela 29 June 2017

Outlook

- - High voltage power supply.
- - High voltage automatic regulation.
- - Monitor (slow control) interface.
- - Central trigger system.
- - DAQ computer.
- - TRB3.

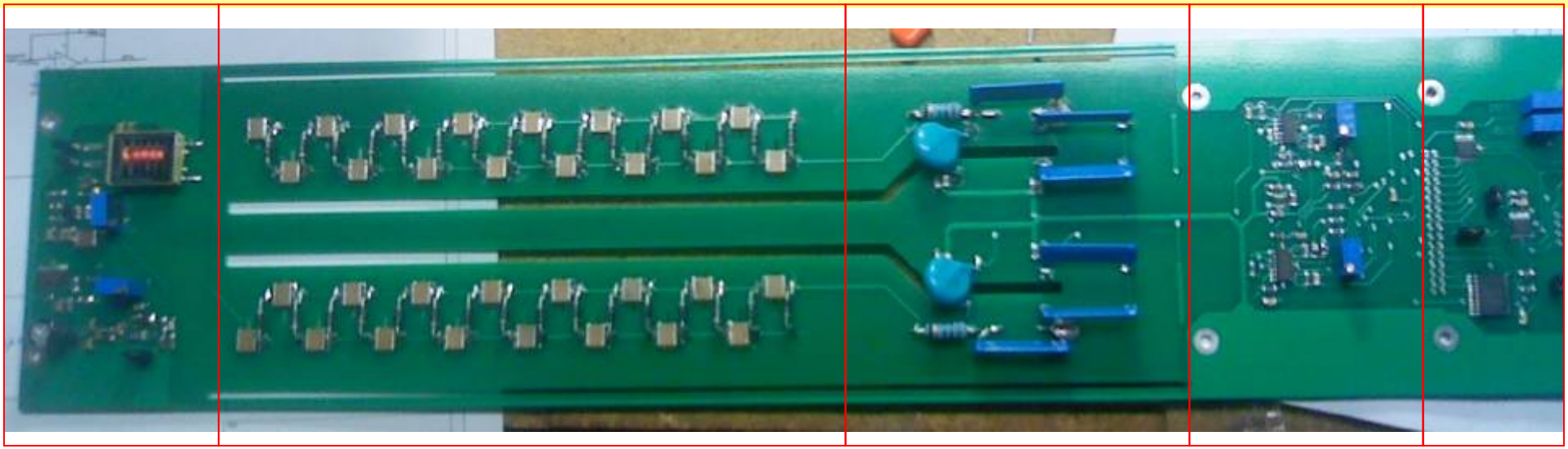
HV power supply. Old design.

Present TRAGALDABAS HV PS



- HV (up to +/- 7kV) not regulated.
- **Based on DC-DC converters (EMCO E70R). Expensive. Only available in USA.**
- Monitoring (T,P, %RH sensors) are integrated on the PS.
- High power compsumtion (around 19W).
- Overcurrent protection.
- Voltage and current measurement/channel.
- Supply from 19 V.
- Fully remotely controllable.

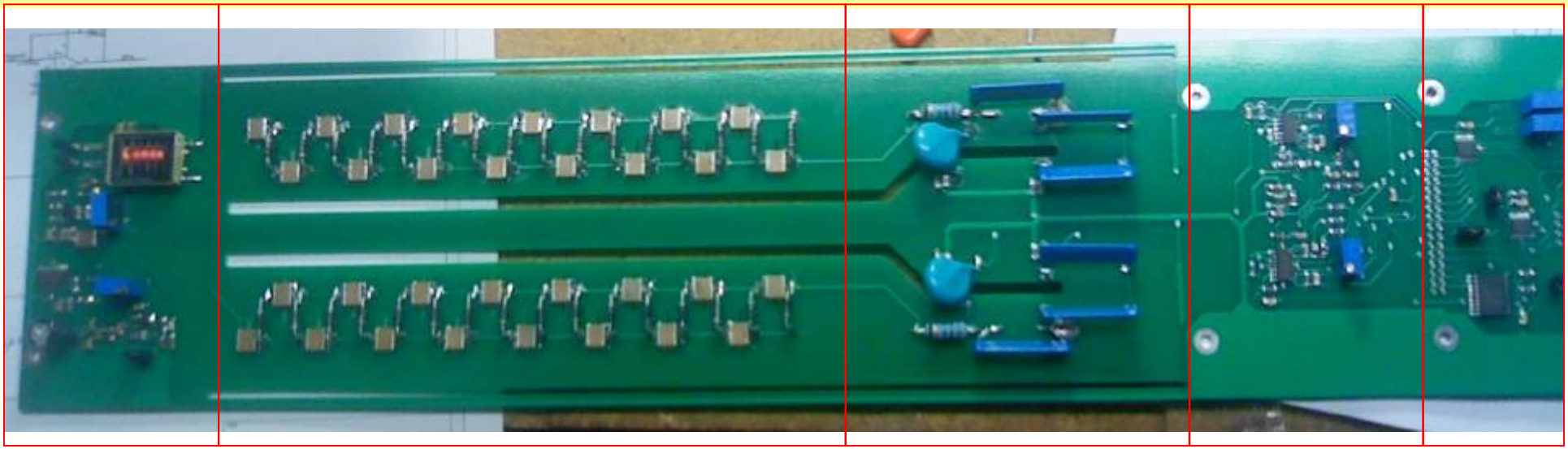
HV power supply. New design.



Control & Oscillator | Dual 16-stage multiplier | Filtering HV output | Measurement | Digital interf. (I^2C)

- **- Regulation of the sum of both polarities up to +/-9kV.**
- **- All components locally available.**
- - Low power consumption
- **- Voltage (~1V precision) and current (~0.1nA precision) measurement/channel**
- - Over-current protection in each channel (common setting)
- - Internal humidity check (by measuring leakages in the PCB)
- - Supply from 5V to 36V
- - Fully remotely controllable (I^2C interface).

HV power supply. New design.



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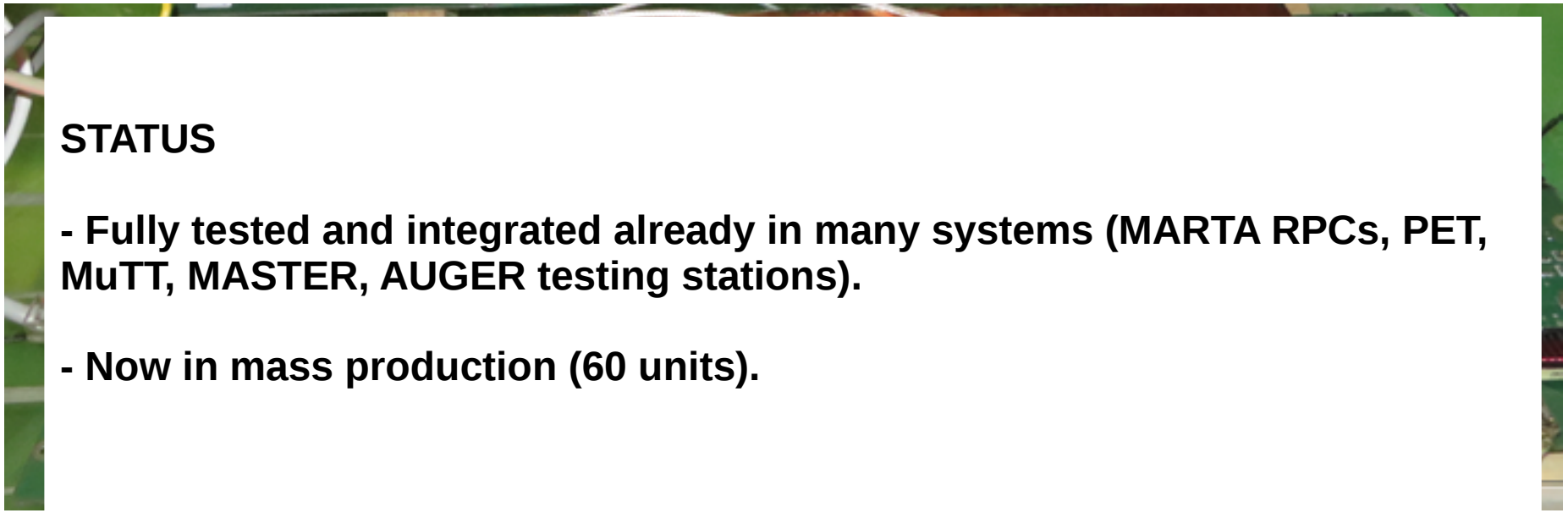
HV power supply

HV power supply fully potted and shielded. Under test.



STATUS

- Fully tested and integrated already in many systems (MARTA RPCs, PET, MuTT, MASTER, AUGER testing stations).

- Now in mass production (60 units).

- F
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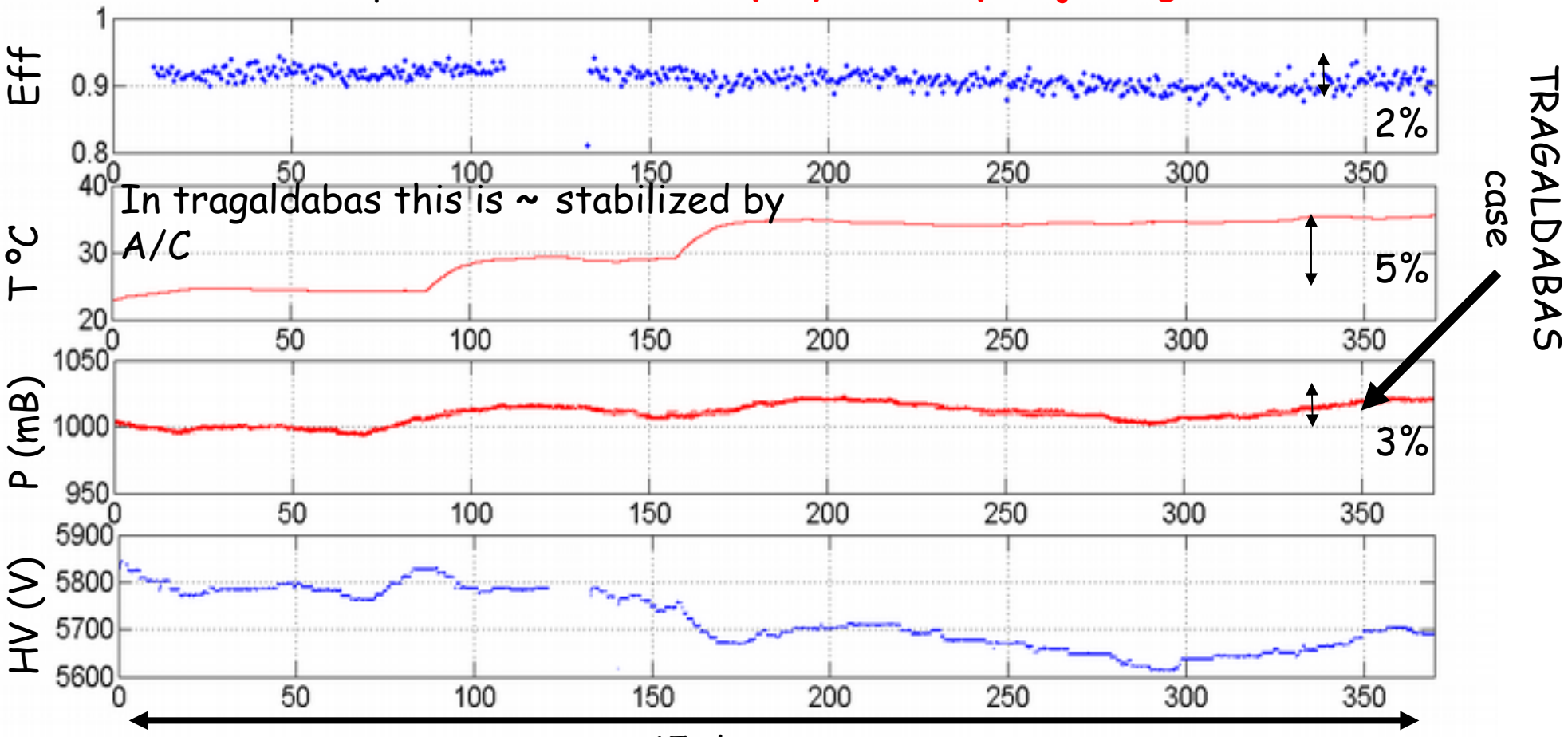
HV power supply. Automatic regulation

Tested in a similar setup

Efficiency is kept stable (+- 1%) for temperature excursion of 15°C and natural pressure variations **by dynamically adjusting the HV**.



Gaseous electronics => $\delta HV/HV = -\delta T/T = \delta P/P$

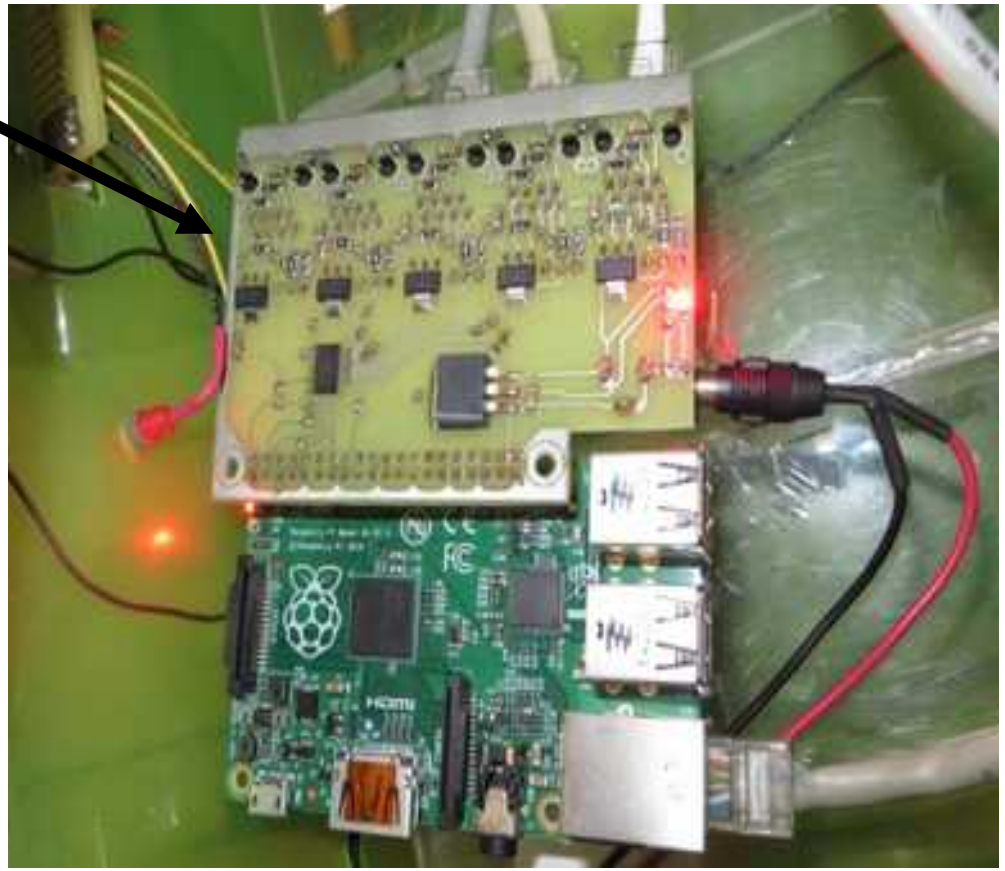
Monitoring interface

Present TRAGALDABAS **monitoring (T, P, %RH sensors) is included on the HV PS**
This is **based on a u-controler => modifications of the functionality are difficult**
=> **decouple both thing** (HV PS and monitoring).

Rasperry PI + I^2C multiplexer

- Up to 8 I^2C buses (more are also possible)
- **Programed in high level: C++**
- **Fully remotely updatable**
- I^2C bus arbitration embebed on the kernell
- **Inexpensive**

-Currently implemented:
  - T sensors
  - P sensors
  - %RH sensors
  - HV PS
  - Some DACs and ADCs



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- There is also a low power consumption version.

- It is also in mass production (60 units).

Rasper

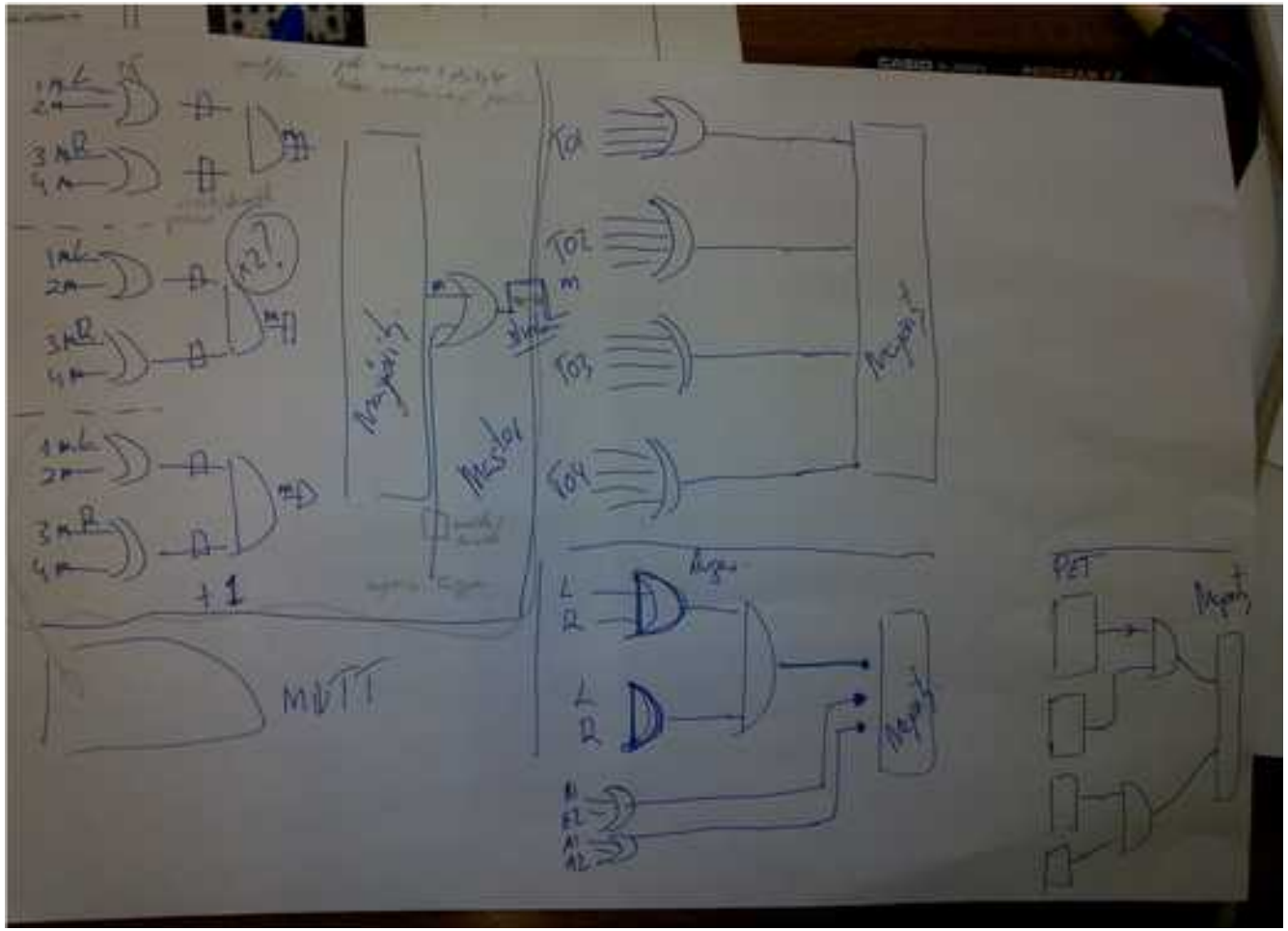
- Up to
- Progr
- Fully
- I²C b
- Inex

-Curre
- T
- P
- %
- H
- S

Central trigger system

IDEA: replace the present trigger system based in expensive, bulky, unflexible NIM modules by a FPGA based unit.

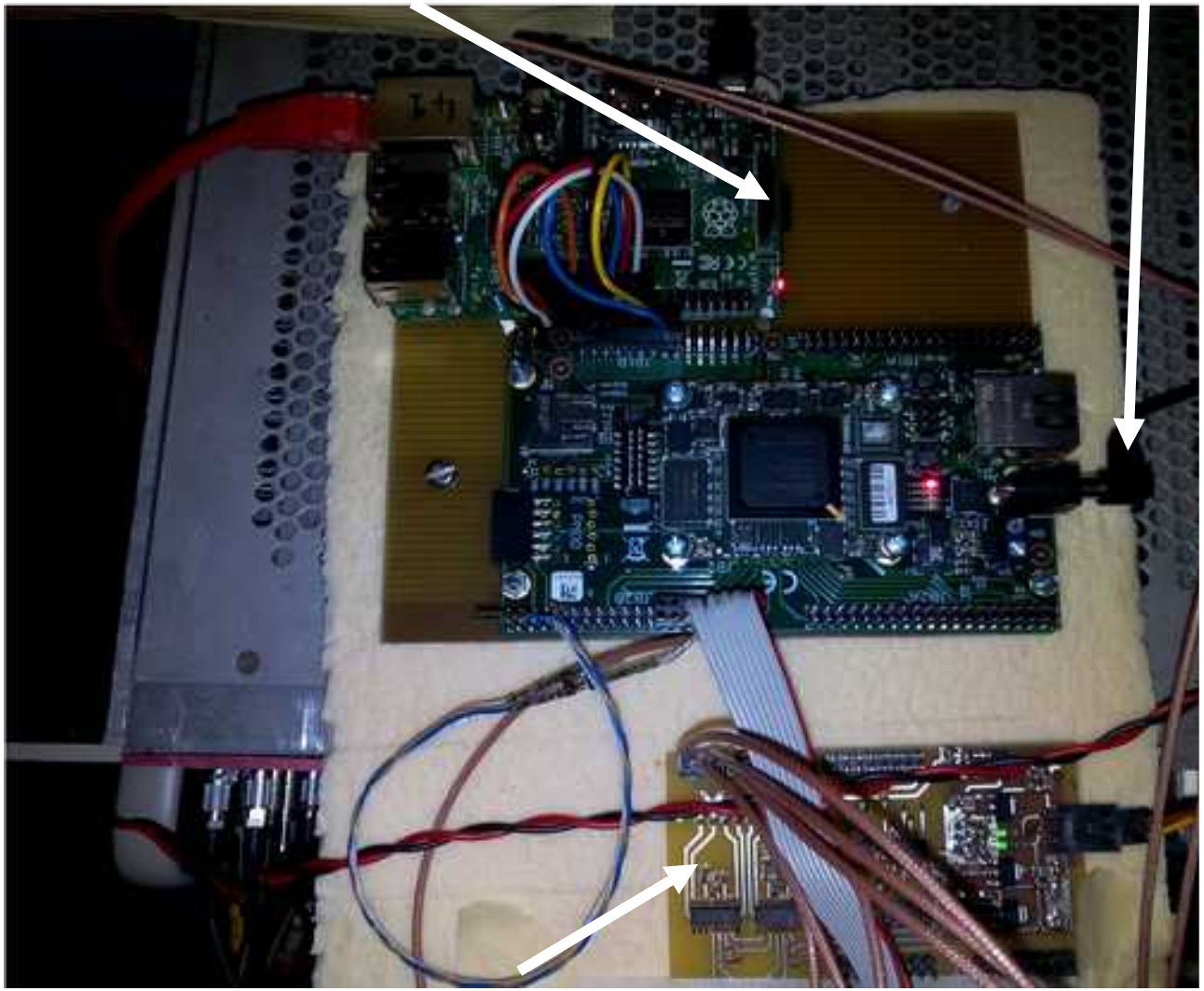
Versatile implementation of different trigger schemes.
Cover all the possible setups that exist right now.



Central trigger system

RaspberryPi for comunication and interface

FPGA (XILIX spartan 6) development board



Interface detector - FPGA

Central trigger system

RaspberryPi for comunication and interface

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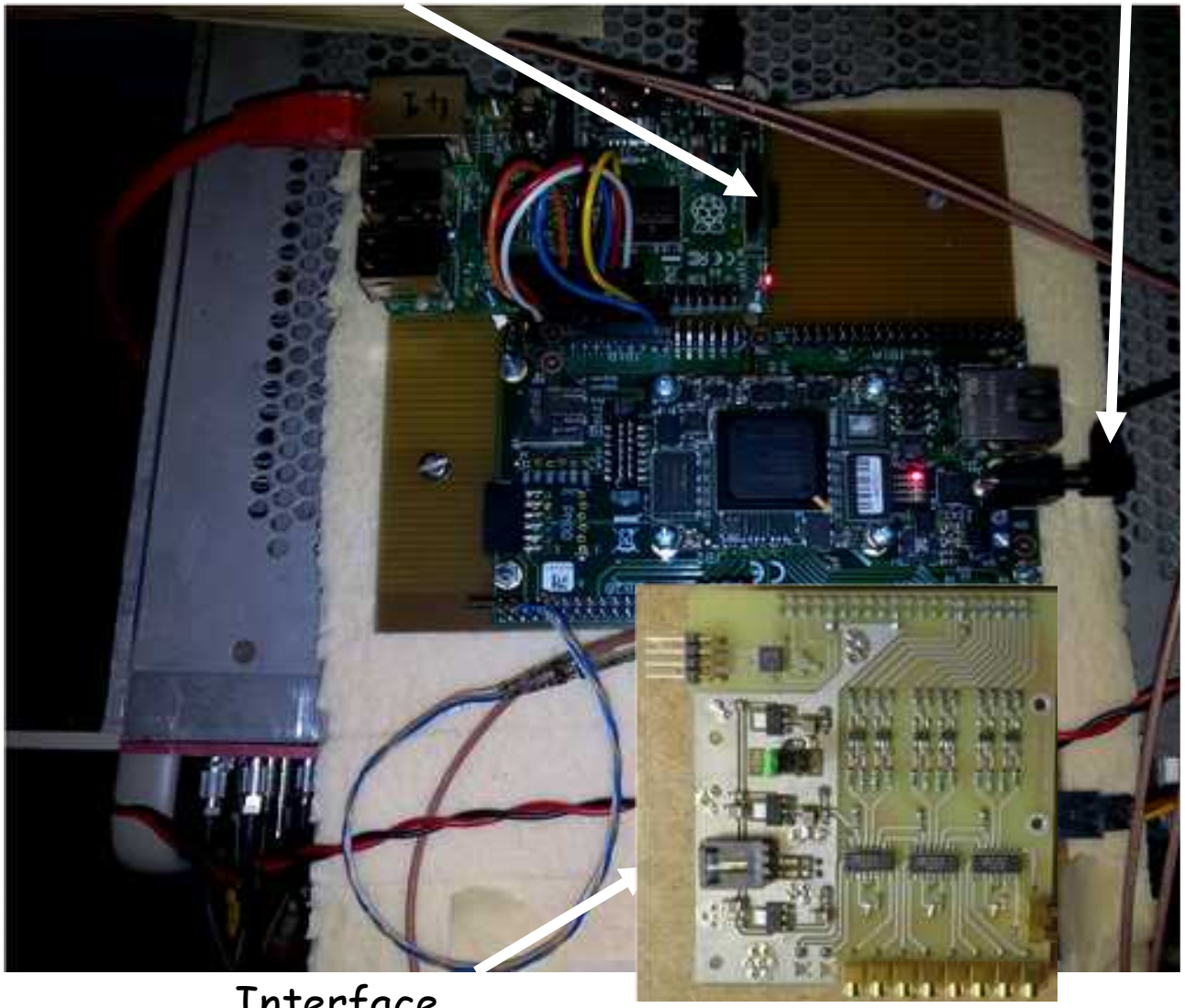

Interface detector - FPGA

Functionality:

-Fully remotely configurable

Input
- 32 NIM/TTL/LVTTL
- Monitoring + log (scalers)

Logic
- Arbitrary And / Or (two stages) + majority
- Internal clock

Output
- 4 LVDS
- Delay / streching

Central trigger system

RaspberryPi for comunication and interface

FPGA (XILIX spartan 6)

STATUS

- Many other features has been implemented mean while.

gurable

- Selectable time width of the inputs.
- Internal monitoring of the signal in the logic blocks.
- Possibility to bypass the inputs directly to the DAQ (proper electronic format of the signals), with good timing qualities.

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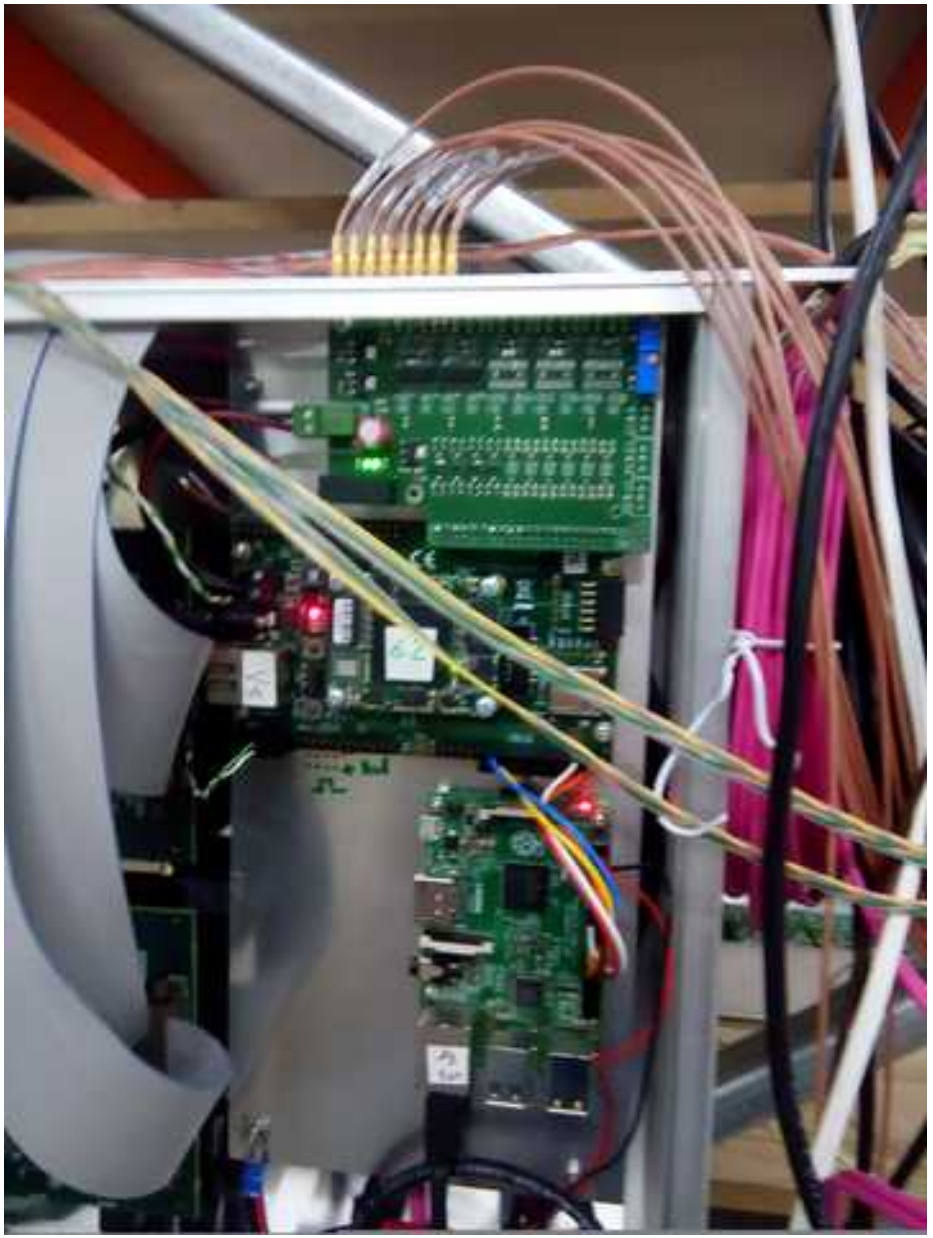
alers)

- The limit is in our imagination.

(two

Interface detector - FPGA

Central trigger system



- Already integrated in many systems. MASTER, MuTT, PET.

- It will be integrated and tested in AUGER testing station (Coimbra telescope) before installation in TRAGALDABAS

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- It replace expensive and bulky NIM electronics.

DAQ computer

- Raspberry like computers are now integrated as DAQ computer.

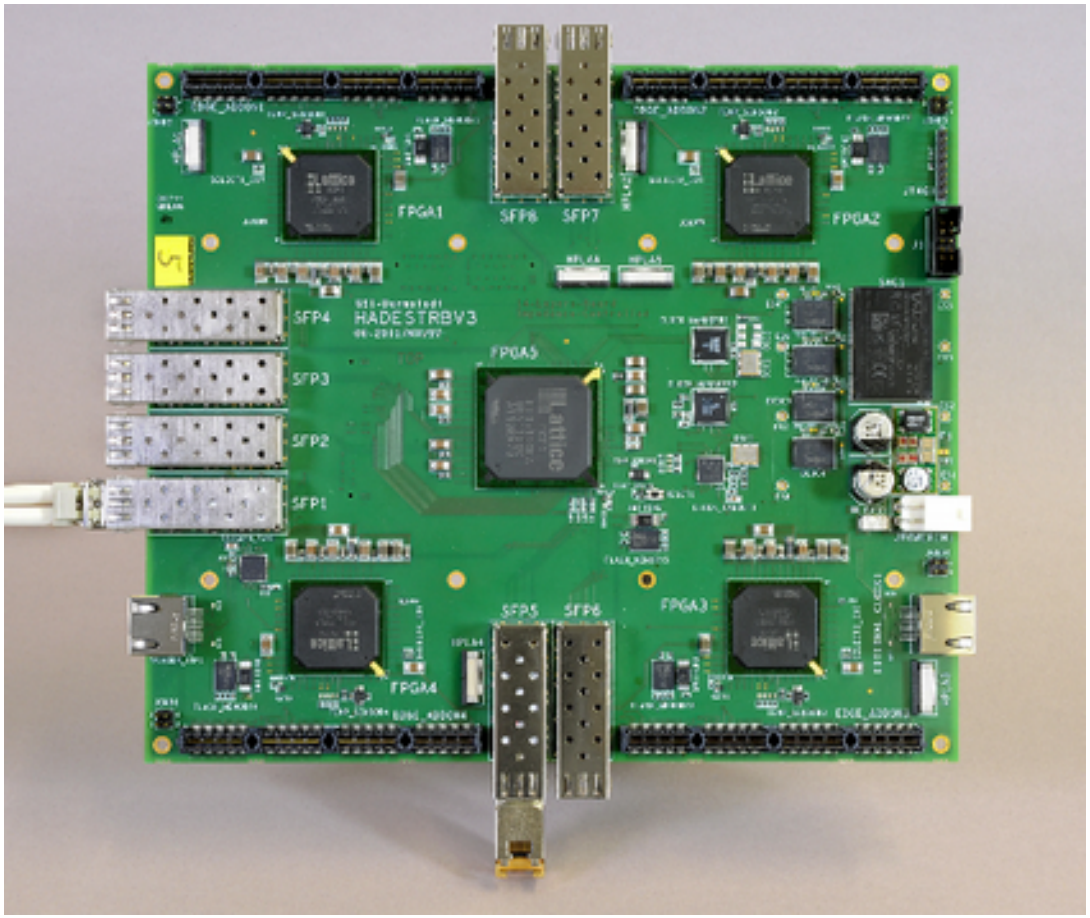
- Inexpensive (50 €) and easy to replace.

- Already tested in few setups and test beams.

- Quite performing. Capable of reading up to ~500 Mbits

TRB3

Evolution of the TRB2



One central FPGA with trigger management capabilities and comunications plus 4 sockets with capability to operate.

- Multi-hit TDC
- ADCs channels @ 40 Mhz
- Data concentrators
- PADIWA amps
- …

And much more

A Neiser *et al* 2013 *JINST* **8** C12043
doi: 10.1088/1748-0221/8/12/C12043

TRB3 Vs TRB2

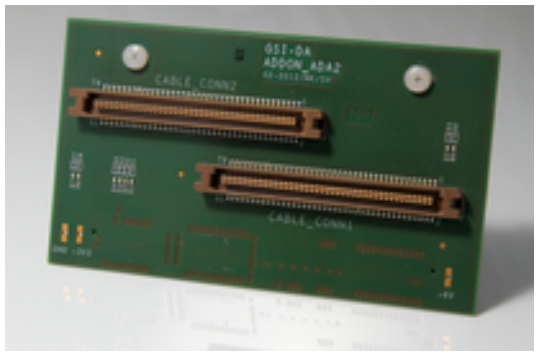
TRB2

- It is **no longer supported or available** (HPTDC chips do not exist any longer).
- **Present setup is a "bricolage"**. Boards are running without any kind of synchronization, which is granted by couple of "tricks". **=> extra dead time and low duty cycle.**

TRB3

- **Full support and availability.**
- **Compatible** (a priory) with HADES-RPC FEE through the 80PIN-Addon, to be check.
- 130 double edge channels/TRB3
- Time resolution down to 20 ps sigma.
- Trigger management capability and board synchronization.

80PIN-Addon



Change to TRB3 will imply.

- **Money**. 2500 € / plane (TRB3)+ 3000 € CTS + network concentrator.
- **Small software modifications**, unpacker and SPI (threshold setting).

Central trigger System